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REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-76 remain in the application. Claims 1-38 are subject to examination. Claims 39-76 have been withdrawn from examination. Claims 1 and 20 have been amended.

On page 2 of the above-identified Office Action, while claims 1 and 20 were not expressly rejected under 35 U.S.C § 112, second paragraph, it is presumed this was an inadvertent oversight on the part of Examiner. Accordingly, applicant will treat those claims as if they were so rejected. In item 3 on page 2 of the above-identified Office action, the Examiner states that the phrase "such as" renders claims 1 and 20 indefinite presumably under 35 U.S.C. § 112, second paragraph and refers to MPEP 2173.05(d).

More specifically, the Examiner states that it is not clear whether the limitations following the phrase "such as" are part of the claimed limitations.

Claims 1 and 20 have been amended to clarify that the claimed structural hardware unit is configured like PLAs, GLAs, PLDs, FPGAs. The claims do not necessarily specifically include the

latter items. Rather, the claims recite that the configuration of the claimed structural hardware unit has a configuration like them.

Support for these changes may be found in the original claims of the instant application and on page 25, lines 4-9 of the specification of the instant application.

It is accordingly believed that the claims meet the requirements of 35 U.S.C. § 112, second paragraph. The above noted changes to the claims are provided solely for clarification or cosmetic reasons. The changes are not provided for overcoming the prior art.

In item 5 on page 3 of the above-identified Office Action, claims 1-7, 10-11, 13-26, 29-30, and 32-38 have been rejected as being unpatentable over Moore et al. (US 6,598,148) (hereinafter referred to as "Moore") in view of Muthujumaraswathy et al. (US 6,279,045) (hereinafter referred to as "Muthujumaraswathy") under 35 U.S.C. § 103(a).

In item 22 on page 9 of the above-identified Office Action, claims 8, 9, 12, 27, 28, and 31 have been rejected as being unpatentable ove Moore in view of Muthujumaraswathy, and further in view of Takahashi et al. (US 5,825,878)

(hereinafter referred to as "Takahashi") under 35 U.S.C. § 103(a).

As will be explained below, it is believed that the claims were patentable over the cited art in their previously presented form and, therefore, the claims have not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a program-controlled unit, having:

a plurality of units selected from the group consisting of internal peripheral units disposed inside the program-controlled unit, external peripheral units exterior to the program-controlled unit, and one or more memory devices;

a structurable hardware unit selectively forming an application-specifically configurable intelligent interface for respectively connecting said intelligent core and said units, including at least one of an interface connection between said intelligent core and said internal peripheral units, an interface connection between said intelligent core and said external peripheral units, an interface connection

between said intelligent core and said memory devices, and an interface connection between said plurality of units; and

said structurable hardware unit being configured like a configuration of field-programmable logic arrangements including PLAs, GLAs, PLDs, or FPGAs and to evaluate and process data and/or signals received. (emphasis added)

Moore discloses a microprocessor integrated circuit having a processing unit located on an integrated circuit substrate. The processing unit operates according to a predefined set of program instructions, which are stored in an instruction register. The integrated circuit also has a memory for storing information provided by the processing unit. The substrate also has a ring oscillator thereon. The microprocessor 50 multiplexes the address/data bus by using a feedback to allow the processor to adjust memory bus timing to be fast with small loads and slower with large loads. The output enable line 152 from the microprocessor 50 is connected to all the memories 150 on the circuit board and the loading on the enable line 152 to the microprocessor 50 is directly related to the number of memories 150 connected. The microprocessor monitors how rapidly line 152 goes high after a read and thus, is able to determine when the data hold time has been satisfied and place the next address on the bus. The

microprocessor generates the system clock and clock circuit 430 tests process performance. The clock is disposed on the same chip as the microprocessor. There is no apparent disclosure in Moore of the interface connection between the intelligent core (shown as microprocessor 11 in the present application) and the various internal and external peripheral units and the memory devices with the structurable hardware unit (shown as SLE layer 12 in the present application) being configured as recited in the instant claims. It is not at all apparent from the disclosure in Moore that there is an independent access according to the present invention. According to the present invention, the layer 12 can transfer data from and to the memory devices independently, that is, without the participation of the microprocessor, which is not shown in Moore. Nor does Moore disclose a NAND or a sub-block configured as a state machine for central sequence control as recited in instant dependent claim 12.

Muthujumaraswathy discloses integrated architecture for multimedia processing wherein a single integrated circuit operates as a system or subsystem and is adaptable to processing a variety of multimedia algorithms. The reference shows that user-programmable(reconfigurable) logic such as a field-programmable gate array(FPGA). There is no good reason why one skilled in the art would extract isolated disclosures

and combine them with Moore except for a hindsight reconstruction of the instant claimed invention.

Moreover, applicant respectfully submits that the filing date of Muthujumaraswathy is October 5, 1998. Applicant has shown (in the Response submitted on August 7, 2006 filed in the instant application) that the instant invention was made prior to September 14, 1998, prior to the aforementioned October 5, 1998 filing date of Muthujumaraswathy. The Examiner is attempting to rely on Muthujumaraswathy's provisional application filing date of September 29, 1997 as being the effective reference date of Muthujumaraswathy. However, the Examiner has not shown that Muthujumaraswathy is entitled to September 29, 1997 as an effective reference date. The burden is on the Examiner to show that Muthujumaraswathy is entitled to the earlier date of September 29, 1997 as its effective date as a reference. Applicant does not have ready access to the provisional application and therefore, submits that the Examiner must make a comparison of the disclosures of the provisional application and the Muthujumaraswathy patent, to determine if Muthujumaraswathy is entitled to the earlier date of September 29, 1997 as a reference. If the Examiner is unable to sustain this burden of proof, then Muthujumaraswathy is not available as a reference against the invention as

recited in the claims of the instant application and the rejection of the claims is rendered moot.

Takahashi discloses a secure embedded memory management unit for a microprocessor for data transfer from an external memory. While Takahashi shows the use of NAND gates 56, 60, there is no apparent reason why one skilled in the art would necessarily combine Takahashi with Moore other than through hindsight. There is no teaching or suggestion in Moore that Moore requires or for that matter would even want to use the NANDs shown in Takahashi. Or that Moore has need or would want to use a sub-block configured as a state machine for central sequence control. And even if the combination of Takahashi with Moore is proper, which it is not, the resulting unit still would not result in the claimed invention. Takahashi does not overcome the deficiencies of Moore. The Examiner's statements that it would have been obvious to combine Takahashi with Moore "because it would provide a high performance microprocessor that can be directly connected to memory controller" is nothing more than wishful thinking on the part of the Examiner. It is apparent that the Examiner has recognized the deficiencies of the primary Moore reference relative to the claimed invention and as a consequence then has sought those particular features in the prior art without any motivation or suggestion in Moore.

The references do not show a "a structurable hardware unit selectively forming an application-specifically configurable intelligent interface for respectively connecting said intelligent core and said units" and "said structurable hardware unit being configured like a configuration of field-programmable logic arrangements including PLAs, GLAs, PLDs, or FPGAs and to evaluate and process data and/or signals received" as recited in claim 1 of the instant application. Independent claim 20 contains similar limitations.

It is well settled that almost all claimed inventions are but novel combinations of old features. The courts have held in this context, however, that when "it is necessary to select elements of various teachings in order to form the claimed invention, we ascertain whether there is any suggestion or motivation **in the prior art** to make the selection made by the applicant". Interconnect Planning Corp. v. Feil, 227 USPQ 543, 551 (Fed. Cir. 1985) (emphasis added). "Obviousness can not be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination". In re Bond, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). "Under Section 103 teachings of references can be combined **only** if there is some suggestion or incentive to do so." ACS Hospital Systems,

Inc. v. Montefiore Hospital et al., 221 USPQ 929, 933, 732 F.2d 1572 (Fed. Cir. 1984) (emphasis original). "Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form, must nevertheless be **'clear and particular.'"** Winner Int'l Royalty Corp. v. Wang, 53 USPQ2d 1580, 1587, 202 F.3d 1340 (Fed. Cir. 2000) (emphasis added; citations omitted); Brown & Williamson Tobacco Corp. v. Philip Morris, Inc., 56 USPQ2d 1456, 1459 (Fed. Cir. Oct. 17, 2000). Applicants believe that there is no "clear and particular" teaching or suggestion in Moore to incorporate the features of Takahashi, as proposed by the Examiner.

In establishing a *prima facie* case of obviousness, it is incumbent upon the Examiner to provide a reason why one of ordinary skill in the art would have been led to modify a prior art reference or to combine reference teachings to arrive at the claimed invention. Ex parte Clapp, 227 USPQ 972, 973 (Bd. Pat. App. & Int. 1985). To this end, the requisite motivation must stem from some teaching, suggestion, or inference in the prior art as a whole or from the knowledge generally available to one of ordinary skill in the art and not from the ***applicant's*** disclosure. See, for example, Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1052, 5 USPQ2d 1434, 1439 (Fed. Cir. 1988), *cert. den.*, 488 U.S. 825

(1988). The Examiner has not provided the requisite reason why one of ordinary skill in the art would have been led to modify Moore or to combine Moore's and Muthujumaraswathy and Takahashi's teachings to arrive at the claimed invention. More than a general statement is required to substantiate the combination of references.

Applicant respectfully believes that any teaching, suggestion, or incentive possibly derived from the prior art is only present with hindsight judgment in view of the instant application. "It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps.... The references **themselves** must provide some teaching whereby the applicant's combination would have been obvious." In re Gorman, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991) (emphasis added). Here, no such teaching is present in the cited references.

The Examiner has not show that there existed a teaching, suggestion, or motivation in the references that would have led a person of ordinary skill in the art to combine the elements in the same way as in the claimed configuration. The Examiner has merely made a general statement that there is

motivation for combining the references, but has not shown where such motivation is present in the cited prior art.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1 or 20. Claims 1 and 20 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well, because they all are ultimately dependent on claim 1 or 20. Additionally, the references do not show the claimed features limitations of dependent claims 8, 10, 12 and of dependent claims 27, 29, and 31.

In view of the foregoing, reconsideration and allowance of claims 1-38 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,

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FDP/lq

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